REMARKS

Claims 1-13, 15-17, 51 and 213-218 are pending in the application.

Claims 14, 18-50 and 52-212 were previously canceled.

Reconsideration and review of the claims on the merits are respectfully requested.

Allowable Subject Matter

Applicants appreciate the Examiner's indication that Claims 51 and 215-218 are allowed, and that Claims 3-7 and 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In response, Applicants submit that each of pending Claims 1-13, 15-17, 51 and 213-218 are patentable based on the following remarks.

Response to Claim Rejection - 35 U.S.C. § 103

Claims 1, 2, 8-13, 213 and 214 are rejected under 35 U.S.C. §103(a) as assertedly being unpatentable over Armbrust et al. (U.S. Patent No. 6,251,775), for the reasons given in the Office Action.

The Examiner cites Armbrust et al. (figure 1) as showing a semiconductor device comprising: an insulating underlayer **10;** a first insulating interlayer **10** [*sic* - **14**] formed on said insulating underlayer, said first insulating interlayer having a groove (in which 11-13 sits); a first silicon-diffused metal layer **13** therein buried in said groove; and a first metal diffusion barrier layer **12** formed on said first silicon-diffused metal layer and said first insulating interlayer.

The Examiner concludes that it would have been obvious to one of ordinary skill in the art to use the insulating underlayer and the first insulating interlayer as "merely a matter of obvious engineering choice" as set forth in the cited case law, asserting that the 35 U.S.C. §103 rejection based on an insulating underlayer and a first insulating interlayer deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

Applicants traverse the rejection.

Applicants claim semiconductor devices and recite, for example, where a first metal diffusion barrier layer is formed on the first silicon-diffused metal layer and the first insulating interlayer. As shown, for example, in Applicants' Figures 5H and 5I, the first metal diffusion barrier layer 109 is formed on the first silicon-diffused metal layer 111 and the first insulating interlayer 103.

On the other hand, Armbrust fails to render obvious the present invention. For example, Armbrust discloses where the groove consists of the wiring pattern 11 (made of Cu), the conductor 12 such as Ta or TaNi, and a silicide layer 13 as an interfacial layer between the wiring pattern and a first insulating interlayer 14 and/or conductive material 18 (see Fig. 1). However, Armbrust fails to disclose that the structural location of the silicide layer 13 is "formed on" the wiring pattern 11 and the first insulating interlayer 14. Instead, Armbrust discloses that the silicide layer 13 is formed on the wiring pattern 11, but that the silicide layer is formed *before or under* the first insulating interlayer 14 (see Fig. 1), and Armbrust discloses that "[a] series of insulating layers is then formed above the silicided layer 13." (see column 4, lines 45-

47). Thus, a skilled artisan would not have been motivated to achieve the present invention based on Armbrust. As Applicants' invention is not "merely a matter of obvious engineering choice" of using multiple pieces in replacing a single piece, Armbrust fails to disclose or render obvious the present invention.

More particularly, in columns 3 and 4 and Fig. 1 of Armbrust et al., the silicide layer 13, unlike the silicon-including metal layer of the subject invention, is uniformly formed in the upper portion of the conductor 11. Thus, the double structure of the conductor 11 and the silicide layer 13 of Armbrust et al. actually corresponds to the double structure of the copper layer 107 and the Cu silicide layer 108 of Fig. 1H of the subject patent application. As a result, since the resistivity of the silicide layer is higher than that of the conductor (Cu), the resistance of a wiring layer is substantially increased. Since the total amount of silicon in the silicon-including metal layer is smaller than the total amount of silicon in the silicide layer, an increase of resistance on the wiring can be suppressed by the invention of the subject application.

That is, the silicon-including metal layer of the present invention is neither disclosed nor suggested by Armbrust et al., and for at least that reason, claim 1 is not obvious over Armbrust et al.

Accordingly, Applicants respectfully request reconsideration and withdrawal of the obviousness rejection.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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